REMARKS

This amendment is being filed in response to the Office Action having a mailing date of August 8, 2005. Claims 2-17 and 19-25 are amended as shown. Claim 1 is canceled herein without prejudice. No new matter has been added. With this amendment, claims 2-25 are pending in the application.

In the Office Action, claims 1-5, 8-20, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Komoike (U.S. Patent No. 6,094,736) in view of Kim (U.S. Patent No. 6,148,426). Claims 24 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Komoike in view of Beauchesne (U.S. Patent No. 4,481,627). Claims 6-7 and 21-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Komoike in view of Kim and in further view of Rapoport (U.S. Patent No. 5,557,619). For the reasons set forth below, the applicant respectfully disagrees with these rejections and request that the pending claims be allowed.

I. Discussion of the Applicant's Disclosed Embodiment(s)

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

An embodiment of the present invention is related to the field of testing an integrated circuit (IC) containing both logic and memory elements. One method for testing an IC involves inputting test data from an Automatic Test Pattern Generator (ATPG) and comparing the output with that of an identical circuit known to be performing correctly. However, when the IC contains one or more internal memory components, the memory components effectively act as a blockage. This is because, in normal operation, the memory contents may not be known and the memory output is determined by the selected address and the contents at that address, resulting in logic up to and including the address inputs being unobservable and logic from the

data outputs onwards being uncontrollable. In short, the present inventor has appreciated that a standard ATPG memory test cannot be performed on an IC containing both logic and memory elements.

To overcome the above-mentioned problems, the prior art discloses various methods to isolate logic from memory when performing tests. In contrast, an embodiment of the present applicant's invention removes the need for isolation by making the memory behave in a predictable manner. For example, selected bit patterns, generated in a preloader, are stored in the memory such that the output of the memory at any time is known and the memory can therefore be modeled by combinational logic and/or as a read-only memory (ROM). The logic components of the IC (separate from the memory) can then be tested using a test pattern without being influenced by unpredictable memory behavior. In an embodiment, the "selected" bit pattern is loaded to the memory before testing and a "test" pattern is used to test the logic components--these two patterns differ in their purpose.

II. Discussion of the Cited References

Komoike describes a switching arrangement that facilitates the testing of a semiconductor IC device including a CPU/logic circuit and a DRAM (memory). The DRAM and CPU/logic circuit are connected via a first wiring, a second wiring provides an input for control signals, and a third wiring allows test data to be entered from an external device. A switching circuit between the wirings allows switching between the test mode and normal operation. During testing of the DRAM (memory), the first connection is disabled so that the DRAM and CPU/logic circuit are disconnected from each other. Test patterns are stored in the DRAM, and the test data is then output from the DRAM to an external device for error checking. Once the memory test is complete, the connection between the CPU/logic and DRAM is reinstated so that the stored test data can be transferred from the DRAM and the CPU/logic can be tested separately from the DRAM/memory. Therefore, Komoike allows memory elements on an IC to be tested separately to the logic components by use of a switching arrangement.

In contrast, an embodiment of the present applicant's invention does not perform a memory test--that is, selected bit patterns are stored in the memory, before testing the logic

components, for the purpose of rendering the output of the memory predictable. It is then possible to test the logic components directly connected to the output of the memory without having to worry about the memory behaving erratically as described above. The test data can be supplied to the whole IC by an ATPG, as it would be when performing a test on a circuit containing no memory components. At no point is the memory in one embodiment of the present applicant's invention actually tested as in Komoike. Indeed in an example embodiment of the present applicant's, once the selected bit pattern has been written to the memory, the memory need not be read by an external device, not even to check that the write was successful.

To supply the missing teachings of Komoike, the Examiner has cited Kim. However, Kim does not disclose, teach, or suggest the features provided by the applicant's embodiment(s).

Kim discloses an apparatus and method for generating memory addresses within a memory built in self-test (BIST) circuit. The BIST circuit contains an internal data generator that generates data to be written to the memory being tested, as well as comparison data for comparison to data read from the memory. The examiner states (second paragraph, page 5 of the Office Action) that it would be obvious to "incorporate a BIST circuit having a data generator as taught by Kim in the semiconductor chip of Komoike, for the purpose of generating data to verify a memory under test."

The applicant respectfully disagrees. It is certainly not the case that combining the teachings of Komoike and Kim would produce the applicant's embodiments. The bit pattern provided to the memory by the applicant's embodiment(s) is not used for testing the memory, unlike the data stored in the memory of Komoike, or the data provided by the internal data generator of Kim.

To further cure the deficiencies of Komoike, the Examiner has cited Beauchesne as disclosing configuring of the memory array to operate, effectively, as a combinatorial logic component. Again, the applicant respectfully disagrees with the Examiner's position.

Beauchesne relates to a means of testing memory components such that all inputs to embedded memory are connected to logic components, the output stages of said logic components can be placed in a high-impedance state. This allows the memory to be isolated and

tested separately to the logic components. Beauchesne does not disclose, teach, or suggest writing a selected bit pattern to a memory so as to make the memory predictable, and further does not make the memory component function as an untested logic component in the way provided by the present applicant's embodiment(s).

III. Discussion of the Claims

Claim 9 has been rewritten in independent form to include recitations from its base claim 1, with claim 1 now canceled without prejudice. Newly independent claim 9 is also amended to recite and clarify the roles of the "selected bit pattern" and the "test pattern." Specifically, independent claim 9 recites "a testing circuit to test the combinational logic components, using a test pattern, after the data generator has input the selected bit pattern to the memory" and "a control to selectively control the memory to behave as a ROM after writing the selected bit pattern to the memory, and while testing the integrated circuit using the test pattern."

These features are not disclosed, taught, or suggested by the cited references, whether singly or in combination. In newly independent claim 9, the term "selected" bit pattern is used to refer to the bit pattern written to the memory for the purpose of rendering the output of the memory predictable, such as a ROM. The recited test pattern used for testing the IC is not the "selected bit pattern" in the memory. As explained above, Komoike and the other references test a memory with their test bit pattern. Accordingly, newly independent claim 9 is allowable.

Independent claim 10 is amended to recite a logic testing circuit configured to "test the operation of the logic elements based on a test bit pattern that is input to the logic elements and that is different from the selected bit pattern present in the memory array." As explained above, the cited references do not provide these features. Accordingly, amended independent claim 10 is allowable.

Independent claim 20 is amended to recite "writing the first bit pattern into a memory," "inputting a second bit pattern, different from the first bit pattern, into the logic to be tested after writing the first bit pattern into the memory," and "testing the logic using the second bit pattern, in a manner that an output of the memory is predictable based on the first bit pattern written therein and is independent of the second bit pattern." As explained above, these features

are not disclosed, taught, or suggested by any of the cited references, whether singly or in combination. Accordingly, amended independent claim 20 is allowable.

Independent claim 24 is amended to recite "inputting to the memory array a first pattern of data bits," "inputting to the logic a second pattern of data bits, different from the first pattern of data bits in the memory array, as part of testing the logic after the first pattern of data bits is input to the memory array," and "receiving output from the memory array during the testing of the logic, the output of the memory array being predictable based on the first bit pattern and being independent of the second bit pattern input to the logic for the testing of the logic." These features are not disclosed, taught, or suggested by any of the cited references, whether singly or in combination. Accordingly, amended independent claim 24 is allowable.

IV. Other Claim Amendments

Claims 5, 8-10, 15, and 19 are amended to clarify that these claims (as well as their related claims) do not fall within the scope of 35 U.S.C. § 112, sixth paragraph. Claims 2-8 are further amended to change their dependency to newly independent claim 9.

Dependent claims 2-8, 11-17, 19, 21-23, and 25 are amended to make their recitations consistent with their base claims, and/or to provide proper antecedent basis, and/or to otherwise place such claims in proper format. All of these dependent claims are now in condition for allowance.

V. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to

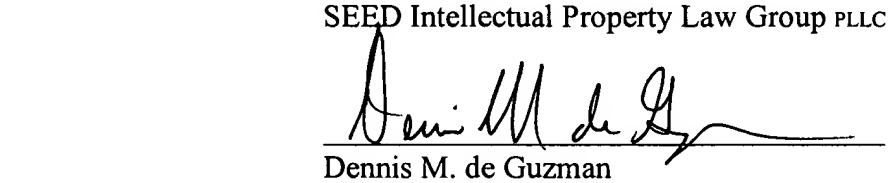
specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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